IN THE SPECIFICATION

Please amend the specification as follows:

Please amend the Title of the Invention at page 1, line 1: IMAGE PROCESSING DEVICE WITH SYNCHRONIZED SPRITE RENDERING AND SPRITE BUFFER

Page 13, line 18 – page 14, line 2:

FIGS. 6A to 6E are timing charts which illustrate the timing of executing the compulsory expansion. As illustrated in FIGS. 6A-6E, ~~When it comes to~~ at the timing [[to]] for reading display data of one line, which is backwardly counted from the start timing of the horizontal display period, under the condition where no expansion access occurs with respect to the sprite buffer 18, in spite of existence or non-existence of an expansion access for the sprite buffer 18, the frame buffer interface 22 compulsorily executes a display access with respect to the frame buffer 23. ~~This is shown in [[time]] the timing charts of FIGS. 6A to 6E, wherein~~ The reference symbol 'DSPLIMIT' shows the compulsory execution timing of the display access described above. Thus, in contrast to FIGS. 5A to 5E, even when no expansion access (see FIG. 6D) may exceptionally occur with respect to the sprite buffer 18, it is possible for the frame buffer interface 22 to execute the display access (see FIG. 6E) for the frame buffer 23 without error.

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